Hall Ticket Number:

Code No. : 14226

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (C.S.E. : CBCS) IV-Semester Main Examinations, January-2021.

Computer Architecture

Time: **2** hours Max. Marks: **60**

*Note: Answer any **NINE** questions from **Part-A** and any **THREE** from **Part-B***

Part-A (9 × 2 = 18 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Calculate the memory space, if a 20-bit address memory has 2*20 memory locations.	2	2	1	2
2.	List out the different addressing modes. What type of addressing mode does Register reference instruction consist of?	2	1	1	1
3.	Register A holds the 8-bit binary 11011001. Determine the B Operand after Left Circular Shift operation.	2	3	2	2
4.	Draw the block diagram for Microprogrammed Control Unit	2	1	2	1
5.	Explain the difference between Cycle Stealing and Burst Transfer	2	1	3	1
6.	Differentiate Isolated , Memory Mapped I/O	2	2	3	1
7.	If there is a magnetic disk system has the following parameters Ts=average time to position the magnetic head over a track, R=rotation speed of disk in revolutions per second, Nt= number of bits per track, Ns= Number of bits per sector, Calculate the average time T, that it will take to read one sector.	2	2	4	2
8.	What is the match logic in Associative Memory?	2	2	5	1
9.	List out the major difficulties which causes the instruction pipeline to deviate from normal operation.	2	1	5	1
10.	Differentiate Data Hazard and Instruction Hazard?	2	2	5	1
11.	A Computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, register code part to specify one of 64 registers and an address part. a) How many bits are there in the operation code, the register code part, and the address part? b) Draw the instruction word format and indicate the number of bits in each part.	2	3	1	2
12.	What is an overflow during arithmetic operations? Explain how it can be detected.	2	3	2	2

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	Part-B (3 × 14 = 42 Marks)				
13. a)	Explain the 16-bit Common bus system with neat diagram.	7	2	1	2
b)	Calculate the effective address for the following instruction R1 has 2000, it follows the indexed addressing mode, MOV 9(R1),LOC	3	3	2	2
c)	Calculate the effective address for the following decimal numbers using 2's complement method A.-67-50 b. 87+34 Note: use binary conversion	4	3	2	2
14. a)	Draw flowchart for Complete computer operation including both instruction and interrupt cycles and Discuss the same.	7	2	2	1
b)	Design Micro program sequencer	7	3	2	2
15. a)	Explain DMA Transfer with a neat diagram	7	2	3	1
b)	Differentiate Programmed I/O and Interrupt Initiated I/O	7	2	3	2
16. a)	Discuss Content Addressable Memory with the help of a neat diagram	7	2	4	1
b)	What is Cache Memory? Explain different types of mapping procedures for cache. A two-way associative cache memory uses blocks of four words. The Cache can accommodate a total of 2048 words from main memory. The main Memory size is 128K/32.What is the size of the cache memory?	7	3	4	2
17. a)	Draw Instruction Pipeline .Discuss the difficulties and solutions for the same.	7	2	5	1
b)	Explain IOP operations in Intel IA-64.	7	2	5	1
18. a)	Evaluate (A*B)+(C*D). Write zero-address, one-address, Two-address and Three-Address Instruction formats.	7	3	1	2
b)	Differentiate Hardwired and Micro Programmed Control Unit	7	2	2	2
19.	Answer any ***two*** of the following:				
a)	Differentiate Strobe control, Handshaking	7	2	3	2
b)	What is Virtual Memory? Explain Paging concept with page table, Associative Page Mapping? A Virtual memory system has an address space of 8K words, a memory space of 4K words, and page and block size of 1K words. The following page reference change occurs during given time interval. 4, 2 , 0 , 1, 2 , 6 , 1 , 4 , 0 , 1, 0 , 2 , 3 , 5 , 7 Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used LRU.	7	3	4	2
c)	Analyse how resource conflict and Data Dependency and Brach Difficulties are addressed in Intel processor to improve the performance	7	3	5	2

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	60.66
2	Knowledge on application and analysis (Level-3 & 4)	39.34
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	--

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